

# 800G OSFP DR8 TRANSCEIVER



### Applications

- Data Center Connectivity: 800G, 8x100G Ethernet connections
- High-Throughput Interconnects: Suitable for cloud and enterprise network architectures
- Telecommunications: Designed for next-generation high-speed networking infrastructure

### **Key Features**

Form Factor: OSFP, hot-pluggable

- Connector Type: Dual MPO-12 (APC)
- High Efficiency: Power consumption <15W
- Temperature Range:  $0^{\circ}\text{C}$  to +70°C case operating (commercial)

Wavelength Range: 1311 nm

Digital Diagnostic Functions: Via I2C interface

Standards Compliance: OSFP MSA Rev 5\_06, IEEE Std

### **Ordering Information**

Form Factor	Data Rate	Media	Distance	Wavelength	TX Power (per lane)	Voltage	DDM	Temperature Range	Part Number
OSFP	800G	SMF	500 m	1331 nm	-2.9 to 4 dBm	3.3 V	Yes	0 to +70 °C	A8SMANQ8EDLA1677

# Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min	Мах	Unit
Storage Temperature	TS	-	-40	+85	°C
Storage Relative Humidity	RH	Non-condensing	5	85	%
Supply Voltage # 3.3	VCC	-	0	3.6	V

# **Absolute Maximum Ratings**

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Operating Temperature (Case)	тс	-	0	-	70	0C
Supply Voltage	VCC	-	3.135	3.3	3.465	V
Power Consumption	Pwr	-	-	-	15	W
Data Rate	DR	-	-	8x100	-	Gbps
Distance		-	0.002	0.5	-	km

# **Electrical Characteristics**

#### Transmitter

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Differential Input Impedance	RDI	-	-	100	-	Ohm
High Speed Differential Input Voltage (CML)	VCML_DI	AC-Coupled, peak-to-peak	0.2	-	0.9	V
Low speed Input Voltage - Low (LVCOMS)	VLVCMOS_IL	-	-0.3	-	Vcc*0.3	V
Low speed Input Voltage - High (LVCOMS)	VLVCMOS_IH	-	Vcc*0.7	-	Vcc+0.5	V
Low speed Input Voltage - Low (LVTTL)	VLVTTL_IL	-	-0.3	-	0.8	V
Low speed Input Voltage - High (LVTTL)	VLVTTL_IH	-	2	-	Vcc+0.3	V

#### Receiver

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Differential Output Impedance	RDO	-	-	100	-	Ohm
High Speed Differential Output Voltage (CML)	VCML_DO	AC-Coupled, peak-to-peak	0.3	-	0.8	V
Low speed Output Voltage - Low (LVCOMS)	VLVCMOS_OL	-	0	-	0.4	V
Low speed Output Voltage - High (LVCOMS)	VLVCMOS_OH	-	Vcc-0.5	-	Vcc+0.3	V
Low speed Output Voltage - Low (LVTTL)	VLVTTL_OL	-	0	-	0.4	V
Low speed Output Voltage - High (LVTTL)	VLVTTL_OH	-	Vcc-0.5	-	Vcc+0.3	V

### **Optical Characteristics**

#### Transmitter

Parameter	Symbol	Conditi ons	Min	Тур	Max	Unit
PAM4 Signaling rate, each lane (range)	-	-	-	53.125±100 ppm	-	GBd
Lane wavelengths (range)	λc	-	1304.5	1311	1317.5	nm
Side Mode Suppression Ratio	SMSR	-	30	-	-	dB
Average launch power, each lane(a)	PO	-	-2.9	-	4	dBm
Outer OMA, each lane(b)	OMA	-	-0.8	-	4.2	dBm
Launch power in OMAouter minus TDECQ, each lane (min)	-	-	-2.2	-	-	dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane	TDECQ	-	-	-	3.4	dB
Average launch power of OFF transmitter, each lane	Poff	-	-	-	-15	dBm
Extinction ratio	ER	-	3.5	-	-	dB
RIN17.10MA	-	-	-	-	-136	dB/Hz
Optical return loss tolerance	-	-	-	-	21.4	dB
Transmitter reflectance(c)	-	-	-	-	-26	dB

#### Receiver

Parameter	Symbol	Conditi ons	Min	Тур	Max	Unit
Modulation format	-	-	-	PAM4	-	-
Lane wavelengths (range)	λc	-	1304.5	1311	1317.5	nm
Damage threshold(d), each lane	-	-	5	-	-	dBm
Average receive power, each lane(e)	-	-	-5.9	-	4	dBm
Receive power (OMAouter), each lane	-	-	-	-	4.2	dBm
Receiver reflectance	-	-	-	-	-26	dB
Receiver sensitivity (OMAouter), each lane(f)	-	-	-	-	-3.9	dBm
Stressed receiver sensitivity (OMAouter), each lane(g)	-	-	-	-	-1.9	dBm
Conditions of stressed receiver sensitivity test:(h)						
Stressed eye closure for PAM4 (SECQ), lane under test	-	-	-	3.4	-	dB
OMAouter of each aggressor lane	-	-	-	4.2	-	dBm

a) Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

b) Even if the TDECQ < 1 dB, the OMAouter (min) must exceed these values

c) Transmitter reflectance is defined looking into the transmitter.

d) The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this aver-age power level. The receiver does not have to operate correctly at this input power.

e) Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

f) Receiver sensitivity (OMAouter), each lane (max) is informative

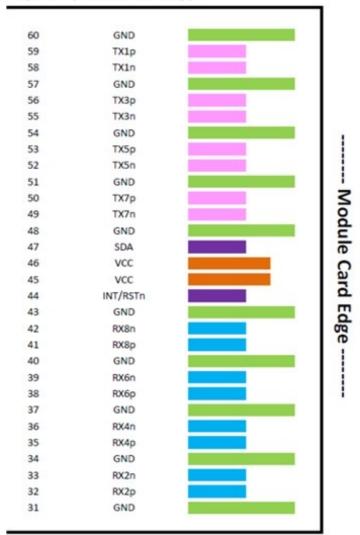
g) Measured with conformance test signal at TP3 (see 124.8.9) for the BER specified in IEEE Std 802.3-2018 clause 124.1.1.

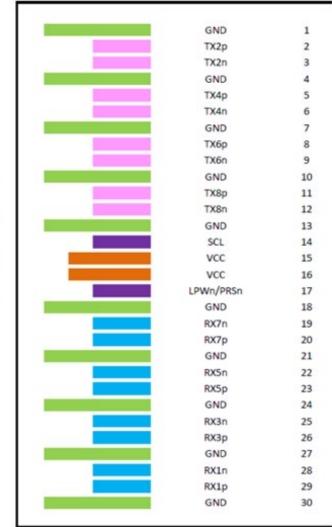
h) These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

# **Pin Description**

### Top Side (viewed from top)

#### Bottom Side (viewed from bottom)







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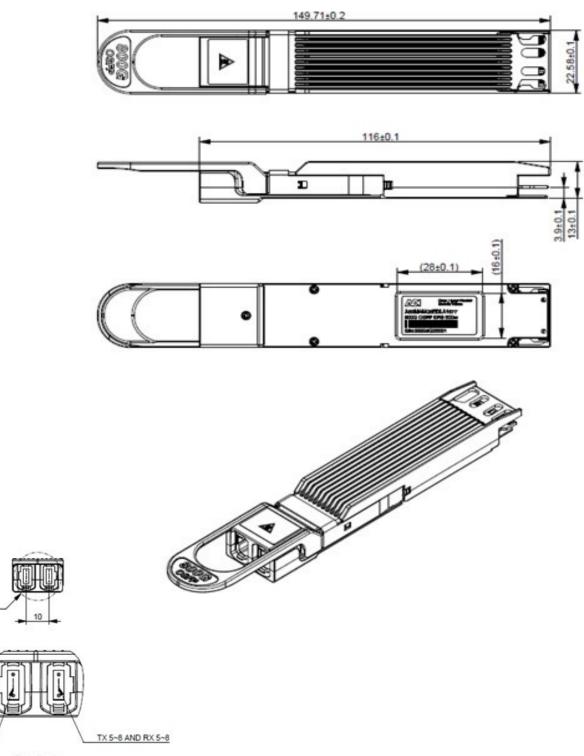
# Pad Function Description

1     GND     Ground     1       2     TX2p     Transmitter Data Non-Inverted     CML-1     Input from Host     3       3     TX2n     Transmitter Data Inverted     CML-1     Input from Host     3       4     GND     Ground     1     1       5     TX4p     Transmitter Data Non-Inverted     CML-1     Input from Host     3       6     TX4n     Transmitter Data Non-Inverted     CML-1     Input from Host     3       7     GND     Ground     1     1       8     TX6p     Transmitter Data Non-Inverted     CML-1     Input from Host     3       9     TX6n     Transmitter Data Non-Inverted     CML-1     Input from Host     3       10     GND     Ground     1     1     1       11     TX8p     Transmitter Data Non-Inverted     CML-1     Input from Host     3       11     TX8p     Transmitter Data Non-Inverted     CML-1     Input from Host     3       12     TX8n     Transmitter Data Non-Inverted     CML-1     Input from Host     3       13     GND     Grou	
A 3TX2nTransmitter Data InvertedCML-IInput from Host34GNDGroundCML-IInput from Host35TX4pTransmitter Data Non-InvertedCML-IInput from Host36TX4nTransmitter Data InvertedCML-IInput from Host37GNDGroundCML-IInput from Host38TX6pTransmitter Data InvertedCML-IInput from Host39TX6nTransmitter Data InvertedCML-IInput from Host310GNDGroundCML-IInput from Host311TX8pTransmitter Data InvertedCML-IInput from Host312TX8nTransmitter Data InvertedCML-IInput from Host313GNDGroundInput from Host3Up resistor on International Interface clockLVCMOS-I/OBi-directional314SCL2-wire Serial interface clockLVCMOS-I/OBi-directional3See pin description Internation Intern	
4GNDGroundInput15TX4pTransmitter Data Non-InvertedCML-IInput from Host36TX4nTransmitter Data InvertedCML-IInput from Host37GNDGroundInput from Host38TX6pTransmitter Data InvertedCML-IInput from Host39TX6nTransmitter Data InvertedCML-IInput from Host310GNDGroundCML-IInput from Host311TX8pTransmitter Data Non-InvertedCML-IInput from Host312TX8nTransmitter Data Non-InvertedCML-IInput from Host313GNDGroundInput from Host3Input from Host314SCL2-wire Serial Interface clockLVCMOS-I/OBidirectional3Open-Drain with Input from Host15VCC+3.3V PowerPower from Host2Input from Host3See pin description in Input from Host316VCC+3.3V PowerPower from HostInput from Host3See pin description in Input from Host3See pin description in Input from Host317LPWn/PRSnLow-Power Mode / Module PresentMulti-LevelBidirectional3See pin description in Input from Host318GNDGroundCML-OOutput to Host3Input from Host319RX7nReceiver Data InvertedCML-OOutput to Host3 </td <td></td>	
5TX4pTransmitter Data Non-InvertedCML-IInput from Host36TX4nTransmitter Data InvertedCML-IInput from Host37GNDGround-18TX6pTransmitter Data InvertedCML-IInput from Host39TX6nTransmitter Data InvertedCML-IInput from Host310GNDGround-111TX8pTransmitter Data InvertedCML-IInput from Host311TX8pTransmitter Data InvertedCML-IInput from Host312TX8nTransmitter Data InvertedCML-IInput from Host313GNDGround-114SCL2-wire Serial Interface clockLVCMOS-I/OBi-directional315VCC+3.3V PowerPower from Host-2up resistor of the sector of the	
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7GNDGroundCML-1Input from Host18TX6pTransmitter Data Non-InvertedCML-1Input from Host39TX6nTransmitter Data InvertedCML-1Input from Host310GNDGroundCML-1Input from Host311TX8pTransmitter Data InvertedCML-1Input from Host312TX8nTransmitter Data InvertedCML-1Input from Host313GNDGroundCML-1Input from Host314SCL2-wire Serial interface clockLVCMOS-I/OBi-directional315VCC+3.3V PowerPower from Host2up resistor on I16VCC+3.3V PowerPower from Host3See pin description17LPWn/PRSnLow-Power Mode / Module PresentMulti-LevelBi-directional318GNDGroundCML-0Output to Host319RX7nReceiver Data InvertedCML-0Output to Host320RX7pReceiver Data InvertedCML-0Output to Host321GNDGround-1122RX5nReceiver Data InvertedCML-0Output to Host323RX5pReceiver Data InvertedCML-0Output to Host323RX5pReceiver Data InvertedCML-0Output to Host3	
8TX6pTransmitter Data Non-InvertedCML-IInput from Host39TX6nTransmitter Data InvertedCML-IInput from Host310GNDGround-1111TX8pTransmitter Data Non-InvertedCML-IInput from Host312TX8nTransmitter Data InvertedCML-IInput from Host313GNDGround-1-14SCL2-wire Serial interface clockLVCMOS-I/OBi-directional3Open-Drain with15VCC+3.3V PowerPower from Host2up resistor on I116VCC+3.3V PowerPower from HostBi-directional3See pin descrip18GNDGround-2up resistor on I19RX7nReceiver Data InvertedCML-OOutput to Host320RX7pReceiver Data InvertedCML-OOutput to Host321GNDGround-1122RX5nReceiver Data InvertedCML-OOutput to Host323RX5pReceiver Data InvertedCML-OOutput to Host323RX5pReceiver Data InvertedCML-OOutput to Host3	
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10GNDGroundCML-IInput from Host111TX8pTransmitter Data Non-InvertedCML-IInput from Host312TX8nTransmitter Data InvertedCML-IInput from Host313GNDGroundCML-IInput from Host314SCL2-wire Serial interface clockLVCMOS-I/OBi-directional315VCC+3.3V PowerPower from Host2up resistor on I16VCC+3.3V PowerPower from Host2up resistor on I17LPWn/PRSnLow-Power Mode / Module PresentMulti-LevelBi-directional318GNDGroundCML-OOutput to Host319RX7nReceiver Data InvertedCML-OOutput to Host320RX7pReceiver Data InvertedCML-OOutput to Host321GNDGround1122RX5nReceiver Data InvertedCML-OOutput to Host323RX5pReceiver Data InvertedCML-OOutput to Host324GNDGround1125RX5nReceiver Data InvertedCML-OOutput to Host326RX5pReceiver Data InvertedCML-OOutput to Host327GNDGround1128RX5pReceiver Data InvertedCML-OOutput to Host329RX5pReceiver Data InvertedCML-	
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12TX8nTransmitter Data InvertedCML-IInput from Host313GNDGround114SCL2-wire Serial interface clockLVCMOS-I/OBi-directional3Open-Drain with15VCC+3.3V PowerPower from Host2up resistor on I16VCC+3.3V PowerPower from Host2up resistor on I17LPWn/PRSnLow-Power Mode / Module PresentMulti-LevelBi-directional3See pin description18GNDLow-Power Mode / Module PresentMulti-LevelBi-directional3See pin description19RX7nReceiver Data InvertedCML-OOutput to Host3Imput for required cirtic20RX7pReceiver Data InvertedCML-OOutput to Host3Imput for required cirtic21GNDGroundCML-OOutput to Host3Imput for required cirtic22RX5nReceiver Data InvertedCML-OOutput to Host323RX5pReceiver Data Non-InvertedCML-OOutput to Host3	
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15VCC+3.3V PowerPower from Host2up resistor on 116VCC+3.3V PowerPower from Host217LPWn/PRSnLow-Power Mode / Module PresentMulti-LevelBi-directional3See pin description18GNDGround1for required cir19RX7nReceiver Data InvertedCML-OOutput to Host320RX7pReceiver Data Non-InvertedCML-OOutput to Host321GNDGround1122RX5nReceiver Data InvertedCML-OOutput to Host323RX5pReceiver Data Non-InvertedCML-OOutput to Host3	
16VCC+3.3V PowerPower from Host217LPWn/PRSnLow-Power Mode / Module PresentMulti-LevelBi-directional3See pin description18GNDGroundC1for required circle19RX7nReceiver Data InvertedCML-OOutput to Host320RX7pReceiver Data Non-InvertedCML-OOutput to Host321GNDGround1122RX5nReceiver Data InvertedCML-OOutput to Host323RX5pReceiver Data Non-InvertedCML-OOutput to Host3	pull
17LPWn/PRSnLow-Power Mode / Module PresentMulti-LevelBi-directional3See pin description18GNDGround1for required cir19RX7nReceiver Data InvertedCML-OOutput to Host3-20RX7pReceiver Data Non-InvertedCML-OOutput to Host3-21GNDGround-122RX5nReceiver Data InvertedCML-OOutput to Host3-23RX5pReceiver Data Non-InvertedCML-OOutput to Host3-	ost
18GNDGround1for required circle19RX7nReceiver Data InvertedCML-OOutput to Host320RX7pReceiver Data Non-InvertedCML-OOutput to Host321GNDGroundT122RX5nReceiver Data InvertedCML-OOutput to Host323RX5pReceiver Data Non-InvertedCML-OOutput to Host3	
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20RX7pReceiver Data Non-InvertedCML-OOutput to Host321GNDGround1122RX5nReceiver Data InvertedCML-OOutput to Host323RX5pReceiver Data Non-InvertedCML-OOutput to Host3	uit
21GNDGround122RX5nReceiver Data InvertedCML-OOutput to Host323RX5pReceiver Data Non-InvertedCML-OOutput to Host3	
22RX5nReceiver Data InvertedCML-OOutput to Host323RX5pReceiver Data Non-InvertedCML-OOutput to Host3	
23 RX5p Receiver Data Non-Inverted CML-O Output to Host 3	
24 GND Ground 1	
25 RX3n Receiver Data Inverted CML-O Output to Host 3	
26 RX3p Receiver Data Non-Inverted CML-O Output to Host 3	
27 GND Ground 1	
28 RX1n Receiver Data Inverted CML-O Output to Host 3	
29 RX1p Receiver Data Non-Inverted CML-O Output to Host 3	
30 GND Ground 1	
31 GND Ground 1	
32 RX2p Receiver Data Non-Inverted CML-O Output to Host 3	

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Pin#	Symbol	Description	Logic	Direction	Plug Sequen	ce Notes
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	<b>Bi-directional</b>	3	See pin description
45	VCC	+3.3V Power	Power from Host		2	for required circuit
46	VCC	+3.3V Power	Power from Host		2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	<b>Bi-directional</b>	3	
48	GND	Ground			1	Open-Drain with pull
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	up resistor on Host
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	ТХ3р	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

# Mechanical Design Diagram (mm)



Detail A

TX 1~4 AND RX 1~4

# **Regulatory Compliance**

Item	Standard
Electromagnetic Interference (EMI)	FCC Part 15 Class B CE EN55032+EN55035 VCCI CISPR32
ESD (Module case) ESD (Module case) ESD (Electrical connector) RoHS	Contact Discharge EN61000-4-2 criterion B Air Discharge EN61000-4-2 criterion B ANSI/ESDA/JEDEC JS-001 2011/65/EU (EU) 2015/863

#### Transmitter

Feature	Standard	Agency
Laser Eye Safety	CDRH 21 CFR 1040.10 and 1040.11	FDA/CDRH
	except for conformance with IEC 60825-1	
	Ed. 3., as described in Laser Notice No.	
Laser Eye Safety	56 IEC 60825-1, EN 60825-1, EN 60825-	TUV/UL
Electrical Safety	2 IEC 62368-1, UL 62368-1, CSA C22.2	UL/CSA/TUV
	NO.	
	62368-1, EN 62368-1	



# **Manufacturing Locations**

USA 13139 Jess Pirtle Blvd, Sugar Land, TX 77478 Taiwan No.18, Gong 4th Rd., Linkou Dist., New Taipei City China No.88, Qiushi Rd., Wangchun Industrial Park, Ningbo

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